Remarks

The Office Action mailed March 21, 2003 has been carefully reviewed and the following remarks have been made in consequence thereof.

Claims 2-5, 7-11, 13-17, 19-22, 24-26, and 28-31 are now pending in this application. Claim 27 has been cancelled without prejudice, waiver, or disclaimer. Claims 1, 6, 12, 18, and 23 were canceled previously. Claims 2, 3, 7, 13, 17, 19, 24, and 28 have been amended. No new matter has been added. Claims 2-5, 7-11, 13-17, 19-22, and 24-31 stand rejected.

In accordance with 37 C.F.R. 1.136(a), a two-month extension of time is submitted herewith to extend the due date of the response to the Office Action dated March 21, 2003 for the above-identified patent application from June 21, 2003 through and including August 21, 2003. In accordance with 37 C.F.R. 1.17(a)(2), authorization to charge a deposit account in the amount of $410.00 to cover this extension of time request also is submitted herewith.

The rejection of Claims 25-30 under 35 U.S.C. § 112, first paragraph, is respectfully traversed. Although the Office Action suggests that Claims 25 and 28 recite a single DAC to implement a discrete digital mode and analog mode rendering Claims 25-30 as containing subject matter which is not described in a way to enable one skilled in the art to make and/or use the invention, Applicants respectfully submit that Claims 25-30 satisfy Section 112, first paragraph. Applicants respectfully submit that one skilled in the art, after reading the specification in light of the figures, would be able to make and/or use the invention as described in Claims 25 and 28. Specifically, the specification states "To enable the 24 volt positive logic discrete input mode, PU 120, P15V 132, N15V 136, RANGE 140, VOUT 144, DH 124, and DL 128 are set to zero...SPI 158 commands DAC 150 to operate at mid-scale output, and microcontroller 114 detects input data via CP 156" (paragraph 22). Moreover, the specification states, "To enable the zero to ten volt analog input mode, PD 116, PU 120, P15V 132, N15V 136, VOUT 144, DH 124, and DL 128 are set to zero...SPI 158 commands DAC 150 through a successive approximation algorithm" (paragraph 30). Accordingly, Applicants respectfully request that the rejection of Claims 25-30 under Section 112, first paragraph, be withdrawn.

For the reasons set forth above, Applicants respectfully request that the rejection of Claims 25-30 under Section 112, first paragraph, be withdrawn.

The rejection of Claims 2-5, 7-11, 13-17, 19-22, and 24-31 under 35 U.S.C. § 102(e) as being anticipated by Sagues et al. (U.S. 2002/0119706 A1) is respectfully traversed.

Sagues et al. describe a system for making interconnections between an input/output module and a first device and a second device where the system uses standard cables and connectors (abstract). A microprocessor of the system may be programmed to recognize particular input data, included for example in an Ethernet packet on a line (86) containing instruction to transmit the data as an analog signal on a line (94) to a device (96) (paragraph 42). The programming in this case would instruct the microprocessor to direct/convert the data through an apparatus (98) having a digital to analog converter (116) (paragraph 42).

Claim 2 recites a control circuit for configuring at least one I/O module connector pin, the circuit including "at least one port controlling a configuration of the at least one pin, said at least one port comprises at least one of a Pull-Down (PD) port, a Pull-Up (PU) port, a Discrete High (DH) port, a Discrete Low (DL) port, a positive 15 volt (P15V) port, a negative 15 volt (N15V) port, a range (RANGE) port, and a voltage out (VOUT) port, said circuit utilizing a single digital to analog converter (DAC) for each said pin to implement a discrete digital mode and an analog mode".

Sagues et al. does not describe or suggest a control circuit for configuring at least one I/O module connector pin, the circuit including at least one port controlling a configuration of the at least one pin, the at least one port comprises at least one of a Pull-Down (PD) port, a Pull-Up (PU) port, a Discrete High (DH) port, a Discrete Low (DL) port, a positive 15 volt (P15V) port, a negative 15 volt (N15V) port, a range (RANGE) port, and a voltage out (VOUT) port, the circuit utilizing a single digital to analog converter (DAC) for each pin to implement a discrete digital mode and an analog mode.

Moreover, Sagues et al. does not describe or suggest a control circuit utilizing a single digital to analog converter (DAC) for each pin to implement a discrete digital mode and an analog mode. Rather, Sagues et al. describe instructing the microprocessor to direct/convert the

data through an apparatus having a digital to analog converter and transmitting the data as an analog signal on a line to a device. For the reasons set forth above, Claim 2 is submitted to be patentable over Sagues et al.

Claim 3 recites a control circuit for configuring at least one I/O module connector pin, the circuit including "at least one port controlling a configuration of the at least one pin; at least one switch assembly comprising a solid state switch, said at least one port controlling whether a respective said at least one solid state switch is in an open state or a closed state; and a single digital to analog converter (DAC) used for each said pin to implement a discrete digital mode and an analog mode".

Sagues et al. does not describe or suggest a control circuit for configuring at least one I/O module connector pin, the circuit including at least one port controlling a configuration of the at least one pin, at least one switch assembly including a solid state switch, the at least one port controlling whether a respective said at least one solid state switch is in an open state or a closed state, and a single digital to analog converter (DAC) used for each of the said pins to implement a discrete digital mode and an analog mode.

Moreover, Sagues et al. does not describe or suggest a control circuit including a single digital to analog converter (DAC) used for each of the said pins to implement a discrete digital mode and an analog mode. Rather, Sagues et al. describe instructing the microprocessor to direct/convert the data through an apparatus having a digital to analog converter and transmitting the data as an analog signal on a line to a device. For the reasons set forth above, Claim 3 is submitted to be patentable over Sagues et al.

Claims 4 and 5 depend from independent Claim 3. When the recitations of Claims 4 and 5 are considered in combination with the recitations of Claim 3, Applicants submit that dependent Claims 4 and 5 likewise are patentable over Sagues et al.

Claim 7 recites an I/O module including "at least one connector pin; a control circuit comprising a plurality of solid state switches, said solid state switches controlling a configuration of the at least one pin; and a single digital to analog converter (DAC) for each said pin to implement a discrete digital mode and an analog mode".

Sagues et al. does not describe or suggest an I/O module including at least one connector pin, a control circuit including a plurality of solid state switches, the solid state switches controlling a configuration of the at least one pin, and a single digital to analog converter (DAC) for each pin to implement a discrete digital mode and an analog mode.

Moreover, Sagues et al. does not describe or suggest an I/O module including a single digital to analog converter (DAC) for each pin to implement a discrete digital mode and an analog mode. Rather, Sagues et al. describe instructing the microprocessor to direct/convert the data through an apparatus having a digital to analog converter and transmitting the data as an analog signal on a line to a device. For the reasons set forth above, Claim 7 is submitted to be patentable over Sagues et al.

Claims 8-11 depend from independent Claim 7. When the recitations of Claims 8-11 are considered in combination with the recitations of Claim 7, Applicants submit that dependent Claims 8-11 likewise are patentable over Sagues et al.

Claim 13 recites a PLC including "a CPU; an I/O module comprising at least one connector pin and a control circuit comprising a plurality of ports, a configuration of the at least one connector pin determined by an energization state of said ports; and a single digital to analog converter (DAC) for each said connector pin to implement a discrete digital mode and an analog mode".

Sagues et al. does not describe or suggest a PLC including a CPU, an I/O module comprising at least one connector pin and a control circuit including a plurality of ports, a configuration of the at least one connector pin determined by an energization state of the ports, and a single digital to analog converter (DAC) for each connector pin to implement a discrete digital mode and an analog mode.

Moreover, Sagues et al. does not describe or suggest a PLC including a single digital to analog converter (DAC) for each connector pin to implement a discrete digital mode and an analog mode. Rather, Sagues et al. describe instructing the microprocessor to direct/convert the data through an apparatus having a digital to analog converter and transmitting the data as an

analog signal on a line to a device. For the reasons set forth above, Claim 13 is submitted to be patentable over Sagues et al.

Claims 14-17 depend from independent Claim 13. When the recitations of Claims 14-17 are considered in combination with the recitations of Claim 13, Applicants submit that dependent Claims 14-17 likewise are patentable over Sagues et al.

Claim 19 recites a method for configuring at least one connector pin utilizing a control circuit, the control circuit including at least one port, the method including "providing an energization state to the at least one port, controlling a configuration of the at least one connector pin utilizing the energization state of the at least one port, and utilizing a single digital to analog converter (DAC) for each said connector pin to implement a discrete digital mode and an analog mode".

Sagues et al. does not describe or suggest a method for configuring at least one connector pin utilizing a control circuit, the control circuit including at least one port, the method including providing an energization state to the at least one port, controlling a configuration of the at least one connector pin utilizing the energization state of the at least one port, and utilizing a single digital to analog converter (DAC) for each connector pin to implement a discrete digital mode and an analog mode.

Moreover, Sagues et al. does not describe or suggest a method including utilizing a single digital to analog converter (DAC) for each connector pin to implement a discrete digital mode and an analog mode. Rather, Sagues et al. describe instructing the microprocessor to direct/convert the data through an apparatus having a digital to analog converter and transmitting the data as an analog signal on a line to a device. For the reasons set forth above, Claim 19 is submitted to be patentable over Sagues et al.

Claims 20-22 depend from independent Claim 19. When the recitations of Claims 20-22 are considered in combination with the recitations of Claim 19, Applicants submit that dependent Claims 20-22 likewise are patentable over Sagues et al.

Claim 24 recites an I/O module including "at least one connector pin; a control circuit comprising: a plurality of switches controlling a configuration of said at least one pin and at least one port controlling a configuration of a respective at least one switch, an energization state of each said at least one port controlling a state of a respective at least one switch; and a single digital to analog converter (DAC) for each said pin to implement a discrete digital mode and an analog mode".

Sagues et al. does not describe or suggest recites an I/O module including at least one connector pin, a control circuit including: a plurality of switches controlling a configuration of said at least one pin and at least one port controlling a configuration of a respective at least one switch, an energization state of each said at least one port controlling a state of a respective at least one switch, and a single digital to analog converter (DAC) for each said pin to implement a discrete digital mode and an analog mode.

Moreover, Sagues et al. does not describe or suggest an I/O module including a single digital to analog converter (DAC) for each said pin to implement a discrete digital mode and an analog mode. Rather, Sagues et al. describe instructing the microprocessor to direct/convert the data through an apparatus having a digital to analog converter and transmitting the data as an analog signal on a line to a device. For the reasons set forth above, Claim 24 is submitted to be patentable over Sagues et al.

Claim 25 recites an I/O module including "at least one connector pin; and a control circuit comprising a plurality of switches controlling a configuration of said at least one pin, said circuit utilizing a single DAC for each said connector pin to implement a discrete digital mode and an analog mode".

Sagues et al. does not describe or suggest an I/O module including at least one connector pin, and a control circuit comprising a plurality of switches controlling a configuration of the at least one pin, the circuit utilizing a single DAC for each connector pin to implement a discrete digital mode and an analog mode.

Moreover, Sagues et al. does not describe or suggest an I/O module including the circuit utilizing a single DAC for each connector pin to implement a discrete digital mode and an analog

mode. Rather, Sagues et al. describe instructing the microprocessor to direct/convert the data through an apparatus having a digital to analog converter and transmitting the data as an analog signal on a line to a device. For the reasons set forth above, Claim 25 is submitted to be patentable over Sagues et al.

Claims 26 depends from independent Claim 25. When the recitations of Claim 26 are considered in combination with the recitations of Claim 25, Applicants submit that dependent Claim 26 likewise is patentable over Sagues et al.

Claim 28 recites a method for configuring at least one connector pin utilizing a control circuit, the method including "controlling a configuration of the at least one connector pin utilizing a single DAC for each pin of the at least one connector pin to implement a discrete digital mode and an analog mode".

Sagues et al. does not describe or suggest a method for configuring at least one connector pin utilizing a control circuit, the method including controlling a configuration of the at least one connector pin utilizing a single DAC for each pin of the at least one connector pin to implement a discrete digital mode and an analog mode.

Moreover, Sagues et al. does not describe or suggest a method including controlling a configuration of the at least one connector pin utilizing a single DAC for each pin of the at least one connector pin to implement a discrete digital mode and an analog mode. Rather, Sagues et al. describe instructing the microprocessor to direct/convert the data through an apparatus having a digital to analog converter and transmitting the data as an analog signal on a line to a device. For the reasons set forth above, Claim 28 is submitted to be patentable over Sagues et al.

Claims 29-31 depend from independent Claim 28. When the recitations of Claims 29-31 are considered in combination with the recitations of Claim 28, Applicants submit that dependent Claims 29-31 likewise are patentable over Sagues et al.

For the reasons set forth above, Applicants respectfully request that the Section 102 rejection of Claims 2-5, 7-11, 13-17, 19-22, and 24-31 be withdrawn.

In view of the foregoing amendments and remarks, all the claims now active in this application are believed to be in condition for allowance. Reconsideration and favorable action is respectfully solicited.

Respectfully Submitted,

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